

## ADP1149/1149-3.3/1149-5

### FEATURES

- Operation to 48 V Input Voltage
- Ultrahigh Efficiency (Up to 95%)
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over Wide Current Range
- Logic Controlled Micropower Shutdown
- Short Circuit Protection
- Very Low Dropout Operation
- Synchronous FET Switching for High Efficiency
- Adaptive Nonoverlap Gate Drives

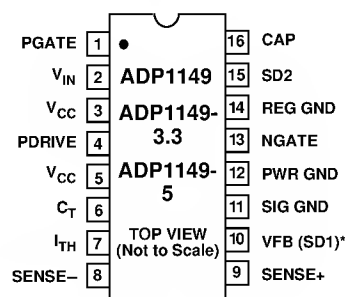
### APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Battery Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

### PIN CONFIGURATIONS

16-Lead Plastic DIP

16-Lead Plastic SO



\*FIXED OUTPUT VERSIONS = SD1

### GENERAL DESCRIPTION

The ADP1149 is a family of synchronous step-down switching regulator controllers featuring automatic-sleep mode to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250 kHz using a constant off-time current-mode architecture.

Special onboard regulation and level-shift circuitry allow operation at input voltages from dropout to 48 V (60 V absolute maximum). The constant off-time architecture maintains constant ripple current in the inductor, easing the design of wide

input range converters. Current-mode operation provides excellent line and load transient response. The operating current level is user programmable via an external current sense resistor.

The ADP1149 incorporates automatic power saving sleep mode operation when load currents drop below the level required for continuous operation. In sleep mode, standby power is reduced to only about 8 mW at  $V_{IN} = 12$  V. In shutdown, both MOSFETs are turned off.

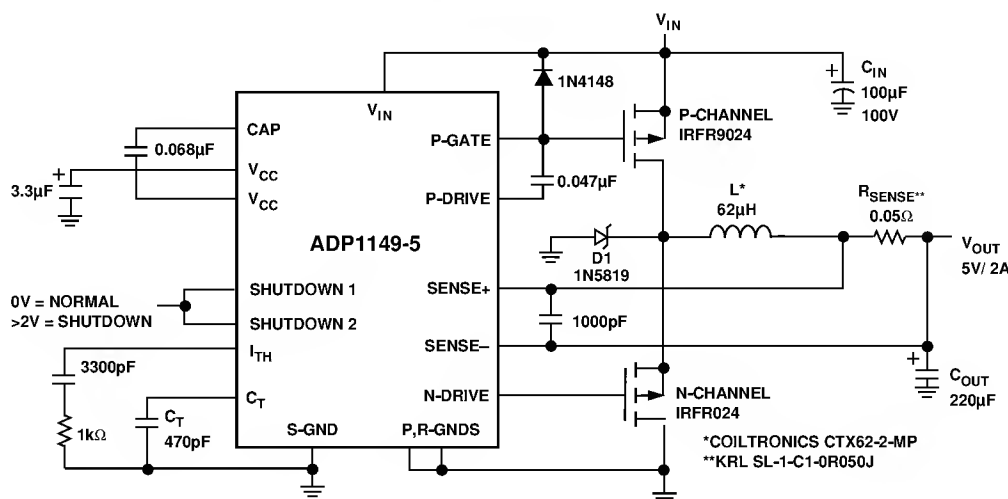


Figure 1. Typical Application

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# ADP1149/1149-3.3/1149-5- SPECIFICATIONS

(@  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{10} = 0\text{ V}$ ,<sup>1</sup>  
unless otherwise noted)

Parameter	Symbol	Conditions <sup>2</sup>	Min	Typ	Max	Units
FEEDBACK VOLTAGE ADP1149 Only*	$V_{10}$	$V_{IN} = 9\text{ V}$	1.21	1.25	1.29	V
FEEDBACK CURRENT ADP1149 Only*	$I_{10}$			0.2	1.0	$\mu\text{A}$
REGULATED OUTPUT VOLTAGE ADP1149-3.3* ADP1149-5*	$V_{OUT}$	$V_{IN} = 9\text{ V}$ $I_{LOAD} = 700\text{ mA}$ $I_{LOAD} = 700\text{ mA}$	3.23 4.9	3.33 5.05	3.43 5.2	V V
OUTPUT VOLTAGE LINE REGULATION	$dV_{OUT}$	$V_{IN} = 9\text{ V to } 48\text{ V}$ , $I_{LOAD} = 700\text{ mA}$	-40		+40	mV
OUTPUT VOLTAGE LOAD REGULATION ADP1149-3.3* ADP1149-5.0*	$dV_{OUT}$	$5\text{ mA} < I_{LOAD} < 2\text{ A}$ $5\text{ mA} < I_{LOAD} < 2\text{ A}$		40 60	65 100	mV mV
SLEEP MODE OUTPUT RIPPLE*	$dV_{OUT}$	$I_{LOAD} = 0\text{ A}$		50		mV p-p
INPUT DC SUPPLY CURRENT* <sup>3</sup> Normal Mode  Sleep Mode  Shutdown	$I_Q$	$V_{IN} = 12\text{ V}$ $V_{IN} = 48\text{ V}$ $V_{IN} = 12\text{ V}$ $V_{IN} = 48\text{ V}$ $V_{IN} = 12\text{ V}$ , $V_{15} = 2\text{ V}$ $V_{IN} = 48\text{ V}$ , $V_{15} = 2\text{ V}$		2 2.2 0.6 0.8 135 300	2.8 3.0 0.9 1.1 170 390	mA mA mA mA $\mu\text{A}$ $\mu\text{A}$
INTERNAL REGULATOR VOLTAGE* (Sets MOSFET Gate Drive Levels)	$V_{CC}$	$V_{IN} = 12\text{ V to } 48\text{ V}$ $I_S = 20\text{ mA}$	9.75	10.25	11	V
$V_{CC}$ DROPOUT VOLTAGE	$V_2 - V_3$	$V_{IN} = 5\text{ V}$ , $I_3 = 10\text{ mA}$		200	250	mV
P GATE TO SOURCE VOLTAGE (OFF)	$V_{IN} - V_1$	$V_{IN} = 12\text{ V}^*$ $V_{IN} = 48\text{ V}^*$	-0.2 -0.2	0 0		V V
CURRENT SENSE THRESHOLD VOLTAGE ADP1149 Only  ADP1149-3.3  ADP1149-5.0	$V_9 - V_8$	$V_8 = 5\text{ V}$ , $V_{10} = 1.32\text{ V}$ (Forced) $V_8 = 5\text{ V}$ , $V_{10} = 1.1\text{ V}^*$ (Forced) $V_8 = 3.5\text{ V}$ (Forced) $V_8 = 2.9\text{ V}$ (Forced)* $V_8 = 5.3\text{ V}$ (Forced) $V_8 = 4.4\text{ V}$ (Forced)*	130 130 130 130 130	25 150 25 150 25 150	170 170 170 170 170	mV mV mV mV mV mV

## NOTES

\*D denotes specifications that apply over the full operating temperature range.

<sup>1</sup>Pin 10 is a shutdown pin on the ADP1149-3.3 and ADP1149-5 fixed output voltage versions and must be at ground potential for testing.

<sup>2</sup> $T_J$  is calculated from the ambient temperature  $T_A$  and power dissipation  $P_D$  according to the following formulas:

ADP1149AR, ADP1149AR-3, ADP1149AR-5:  $T_J = T_A + (P_D \times 110^\circ\text{C/W})$

ADP1149AN, ADP1149AN-3, ADP1149AN-5:  $T_J = T_A + (P_D \times 70^\circ\text{C/W})$

<sup>3</sup>Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. The allowable operating frequency may be limited by power dissipation at high input voltages.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... -15 V to +60 V  
 $V_{CC}$  Output Current (Pin 3) ..... 50 mA  
 $V_{CC}$  Input Voltage (Pin 5) ..... 20 V  
Continuous Output Current (Pins 4, 13) ..... 50 mA  
Sense Voltages (Pins 10, 15) ..... -0.3 V to  $V_{CC}$   
Shutdown Voltages (Pins 10, 15) ..... 7 V  
Operating Temperature Range .....  $0^\circ\text{C to } +70^\circ\text{C}$   
Junction Temperature .....  $+125^\circ\text{C}$   
Storage Temperature Range .....  $-65^\circ\text{C to } +150^\circ\text{C}$   
Lead Temperature (Soldering, 10 sec) .....  $+300^\circ\text{C}$

## ORDERING GUIDE

Model	Output Voltage	Package Description*
ADP1149AN	ADJ	PDIP
ADP1149AR	ADJ	SO-16
ADP1149AN-3.3	3.3 V	PDIP
ADP1149AR-3.3	3.3 V	SO-16
ADP1149AN-5	5 V	PDIP
ADP1149AR-5	5 V	SO-16

\*For outline information see Package Information section.

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